Electronic Version
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Claims

[c1] A method of designing a layout of an alternating phase shifting mask for projecting an image of an integrated circuit design comprising:
providing a design of an integrated circuit layout having a plurality of features to be projected using alternating phase shifting segments, including a feature having a critical width along a length thereof that extends beyond another feature;
providing alternating phase shift design rules based on alternating phase shift design parameters comprising minimum phase width, minimum phase-to-phase spacing, and minimum extension of critical width beyond another feature;
identifying portions of the integrated circuit layout having a critical width feature that violate the alternating phase shift design rules;
redesigning the critical width feature in the integrated circuit layout that violates the alternating phase shift design rules by reducing the length that the critical width feature extends beyond the other feature to the minimum extension; and
generating an alternating phase shifting mask layout

with the reduced length of the critical width feature in conformance with the alternating phase shift design rules.

[c2] The method of claim 1 wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor, and wherein the other feature is a diffusion region of a transistor.

[c3] A method of designing an alternating phase shifting mask for projecting an image of an integrated circuit design comprising:
providing a design of an integrated circuit layout having a plurality of features to be projected using alternating phase shifting segments, including a feature having a critical width along a length thereof;
for each of said features, determining ideal alternating phase shifting segments shapes to be included in an alternating phase shifting mask for projecting the feature;
identifying a conflict between an alternating phase shifting segment shape for the feature having the critical width along a length thereof and another alternating phase shifting segment shape, prior to fabricating the alternating phase shifting mask;
restricting length of the alternating phase shifting segment shape for the feature having the critical width along a length thereof to eliminate the conflict; and

fabricating the alternating phase shifting mask with the restricted length of the alternating phase shifting segment shape for projecting the feature having the critical width along a length thereof.

[c4] The method of claim 3 wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor.

[c5] The method of claim 3 wherein restricting length of the alternating phase shifting segment shape for the gate-shrink region of a transistor comprises reducing the length of the critical width portion of the gate-shrink region.

[c6] The method of claim 3 wherein restricting length of the alternating phase shifting segment shape for the feature having the critical width along a length thereof comprises reducing the length of the critical width portion of the feature.

[c7] The method of claim 3 wherein restricting length of the alternating phase shifting segment shape for the feature having the critical width along a length thereof comprises restricting the length of the critical width portion of the feature in accordance with design rule tolerances.

[c8] The method of claim 7 further including fabricating a

mask with an opaque shape for projecting the portion of the feature length not projected by the restricted length of the alternating phase shifting segment shape.

[c9] The method of claim 3 further including fabricating a mask with an opaque shape for projecting the portion of the feature length not projected by the restricted length of the alternating phase shifting segment shape.

[c10] The method of claim 3 further including restricting length of the other alternating phase shifting segment shape to eliminate the conflict.

[c11] The method of claim 7 further including restricting length of the other alternating phase shifting segment shape to eliminate the conflict.

[c12] The method of claim 3 wherein the other alternating phase shifting segment shape is for projecting a gate-shrink region of a transistor, and further including restricting length of the other alternating phase shifting segment shape to eliminate the conflict.

[c13] The method of claim 4 wherein the other alternating phase shifting segment shape is for projecting a gate-shrink region of a transistor, and further including restricting length of the other alternating phase shifting segment shape to eliminate the conflict.

[c14] The method of claim 5 wherein the other alternating phase shifting segment shape is for projecting a gate-shrink region of a transistor, and further including restricting length of the other alternating phase shifting segment shape to eliminate the conflict.

[c15] The method of claim 4 wherein the gate-shrink region of a transistor to be projected has a portion at the critical width and a portion at a wider, non-critical width, and further including fabricating a mask having an opaque portion to project the non-critical width portion of the gate-shrink region.

[c16] The method of claim 3 wherein the feature having the critical width along a length thereof to be projected has a portion at the critical width and a portion at a wider, non-critical width, and further including fabricating a mask having an opaque portion to project the non-critical width portion of the feature.

[c17] A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for designing a layout of an alternating phase shifting mask, the integrated circuit layout having a plurality of features to be projected using alternating phase shifting segments, in-

cluding a feature having a critical width along a length thereof that extends beyond another feature, the alternating phase shifting mask to be used to project an image of an integrated circuit design, said method steps comprising:

providing alternating phase shift design rules based on alternating phase shift design parameters comprising minimum phase width, minimum phase-to-phase spacing, and minimum extension of critical width beyond another feature;

identifying portions of the integrated circuit layout having a critical width feature that violate the alternating phase shift design rules;

redesigning the critical width feature in the integrated circuit layout that violates the alternating phase shift design rules by reducing the length that the critical width feature extends beyond the other feature to the minimum extension; and

generating an alternating phase shifting mask layout with the reduced length of the critical width feature in conformance with the alternating phase shift design rules.

[c18] The program storage device of claim 17 wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor, and wherein

the other feature is a diffusion region of a transistor.

[c19] An article of manufacture comprising a computer-usable medium having computer readable program code means embodied therein for designing a layout of an alternating phase shifting mask, the integrated circuit layout having a plurality of features to be projected using alternating phase shifting segments, including a feature having a critical width along a length thereof that extends beyond another feature, the alternating phase shifting mask to be used to project an image of an integrated circuit design, the computer readable program code means in said article of manufacture comprising:

computer readable program code means for providing alternating phase shift design rules based on alternating phase shift design parameters comprising minimum phase width, minimum phase-to-phase spacing, and minimum extension of critical width beyond another feature;

computer readable program code means for identifying portions of the integrated circuit layout having a critical width feature that violate the alternating phase shift design rules;

computer readable program code means for redesigning the critical width feature in the integrated circuit layout that violates the alternating phase shift design rules by

reducing the length that the critical width feature extends beyond the other feature to the minimum extension; and

computer readable program code means for generating an alternating phase shifting mask layout with the reduced length of the critical width feature in conformance with the alternating phase shift design rules.

[c20] The article of claim 19 wherein the feature having a critical width along a length thereof comprises a gate-shrink region of a transistor, and wherein the other feature is a diffusion region of a transistor.